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PTO/SB/05 (08-00)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	75622.P0019
First Inventor	HEIN
Title	Low Voltage Sensing and Control of Battery Referenced Transistors in Subscriber Loop Applications
Express Mail Label No.	EL 349960324 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [X] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [*Total Pages* 25] *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (*if filed*)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 6]
5. Oath or Declaration [*Total Pages* 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1 33(b)
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program (*Appendix*)
8. Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all necessary*)
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [X] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: .....
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17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No _____/_____
    Prior application information. *Examiner* _____ *Group / Art Unit* _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

Name	Davis & Johnson, LLP **22503**				
	PATENT TRADEMARK OFFICE				
Address	PO Box 90698				
City	Austin	*State*	TX	*Zip Code*	78709
Country	USA	*Telephone*	(916) 364-1270	*Fax*	(916) 364-1471

Name (Print/Type)	William D. Davis	*Registration No. (Attorney/Agent)*	38,428
Signature	William D. Davis	*Date*	10-21-2000

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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 435

Complete if Known	
Application Number	
Filing Date	October 21,2000
First Named Inventor	HEIN
Examiner Name	
Group Art Unit	
Attorney Docket No.	75622.P0019

METHOD OF PAYMENT

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

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Deposit Account Name

☐ Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17

☐ Applicant claims small entity status See 37 CFR 1 27

2. ☐ **Payment Enclosed:**

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	355
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 355

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below		Fee Paid
Total Claims	20	-20** =	0	X 0	=	0
Independent Claims	4	- 3** =	1	X 40	=	40
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 40

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	710	246	355	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40

SUBMITTED BY				Complete *(if applicable)*	
Name *(Print/Type)*	William D. Davis	*Registration No. (Attorney/Agent)*	38,428	*Telephone*	(916) 364-1270
Signature	William D. Davis			*Date*	10/21/2000

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UNITED STATES PATENT APPLICATION

FOR

LOW VOLTAGE SENSING AND CONTROL OF BATTERY REFERENCED TRANSISTORS IN SUBSCRIBER LOOP APPLICATIONS

INVENTORS:

JERRELL P. HEIN

MARIUS GOLDENBERG

Prepared by:

DAVIS & JOHNSON, L.L.P.
P.O. BOX 90698
AUSTIN, TX 78709
(916) 364-1270

Attorney Docket No. 75622.P0019

EL 349960324 US	October 21, 2000
"Express Mail" mailing label number	Date of Deposit

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LOW VOLTAGE SENSING AND CONTROL OF BATTERY REFERENCED TRANSISTORS IN SUBSCRIBER LOOP APPLICATIONS

FIELD OF THE INVENTION

This invention relates to the field of telecommunications. In particular, this invention is drawn to subscriber loop interface circuitry.

BACKGROUND OF THE INVENTION

Subscriber line interface circuits are typically found in the central office exchange of a telecommunications network. A subscriber line interface circuit (SLIC) provides a communications interface between the digital switching network of a central office and an analog subscriber line. The analog subscriber line connects to a subscriber station or telephone instrument at a location remote from the central office exchange.

The analog subscriber line and subscriber equipment form a subscriber loop. The interface requirements of an SLIC result in the need to provide relatively high voltages and currents for control signaling with respect to the subscriber equipment on the subscriber loop. Voiceband communications are low voltage analog signals on the subscriber loop. Thus the SLIC must detect and transform low voltage analog signals into digital data for transmitting communications received from the subscriber equipment to the digital network. For bi-directional communication, the SLIC must also transform digital data received from the digital network into low voltage analog signals for transmission on the subscriber loop to the subscriber equipment. Strict gain and longitudinal balance control are required for subscriber loop applications.

Multiple high voltage operational amplifiers are frequently used to drive the subscriber loop. The battery feed potential is often used as the negative supply voltage for the operational amplifiers. The operational amplifiers drive the tip and ring voltages of the subscriber loop at levels ranging from ground potential to the battery feed potential, during battery feed and subscriber loop ringing.

One disadvantage of the use of high voltage operational amplifiers is that the operational amplifier bias currents result in non-negligible power losses due to the large potential difference between the positive power supply potential and the battery feed potential. The operational amplifiers are also custom integrated circuits manufactured in a "non-mainstream" high voltage bipolar technology. Yet another disadvantage of this approach is that the operational amplifiers must be closely matched in performance characteristics over a large operating range to ensure proper performance.

SUMMARY OF THE INVENTION

In view of limitations of known systems and methods, a subscriber line interface circuit is described. Generally the tip and ring currents or the departure from the desired tip and ring currents is calculated without direct sensing of either the tip or ring lines of the subscriber loop. These calculated signals are then used to control the tip and ring currents.

A method includes the step of providing subscriber loop pull-down circuitry operating in a first voltage domain. The subscriber loop pull-down circuitry decreases at least one of a tip and a ring line current in response to a corresponding pull-down control signal. The method further includes the step of providing control circuitry operating in a second voltage domain, wherein the first and second voltage domains are substantially distinct. The control circuitry varies the pull-down control signal to vary a selected one of the tip and ring line currents in response to a sensed current corresponding to an associated one of a tip pull-down current and a ring pull-down current.

A subscriber line interface circuit apparatus includes pull-down circuitry to vary line currents of the tip and ring lines in response to a pull-down control signal. The pull-down circuitry operates in a first voltage domain. The apparatus includes control circuitry generating the pull-down control signal. The control circuitry operates in a second voltage domain substantially distinct from the first voltage domain. A control isolation stage is coupled to provide the pull-down control signals from the control circuitry to the pull-down circuitry. A feedback isolation stage provides feedback signals from the pull-down circuitry to the control circuitry. The feedback signals represent

sensed pull-down currents associated with the tip and ring lines. The control circuitry provides the pull-down control signals for the tip and ring lines in response to the sensed pull-down currents.

Other features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

Figure 1 illustrates one embodiment of a central office exchange including a subscriber line interface circuit (SLIC) coupling subscriber equipment to a digital switching system.

Figure 2 illustrates a block diagram of an SLIC including a signal processor and a linefeed driver.

Figure 3 illustrates high voltage precision matched operational amplifiers for driving tip and ring line voltages.

Figure 4 illustrates one embodiment of a linefeed driver circuit.

Figure 5 illustrates current differencing and mirroring circuitry.

Figure 6 illustrates the current differencing and mirroring circuitry used to generate feedback error signals for the tip and ring control circuitry within the signal processor.

DETAILED DESCRIPTION

Figure 1 illustrates functional elements of one embodiment of a subscriber line interface circuit (SLIC) 110 typically associated with plain old telephone services (POTS) telephone lines. The subscriber line interface circuit (SLIC) provides an interface between a digital switching network 120 of a local telephone company central exchange and a subscriber loop 132 including subscriber equipment 130.

The subscriber loop 132 is typically used for communicating analog data signals (e.g., voiceband communications) as well as subscriber loop "handshaking" or control signals. The analog data signals are typically on the order of 1 volt peak-to-peak (i.e., "small signal"). The subscriber loop control signals typically consist of a 48 VDC offset and an AC signal of 40-140 Vrms (i.e., "large signal"). The subscriber loop state is often specified in terms of the tip 180 and ring 190 portions of the subscriber loop.

The SLIC is expected to perform a number of functions often collectively referred to as the BORSCHT requirements. BORSCHT is an acronym for "battery feed," "overvoltage protection," "ring," "supervision," "codec," "hybrid," and "test."

Recent transformerless SLIC designs tend to distribute the functional requirements between two integrated circuits based on whether the functions are traditionally associated with the high voltage subscriber loop controls or the low voltage data processing. For example, in one embodiment, the codec is implemented in a low voltage integrated circuit and the remaining functions (e.g., supervision) are implemented primarily in a high voltage integrated circuit such as a bipolar integrated circuit. Although this design tends to offer considerable space, weight, and power efficiencies over designs

requiring passive inductive components, this distribution of the functional requirements tends to result in a relatively expensive high voltage integrated circuit.

Figure 2 illustrates one embodiment of a SLIC wherein the BORSCHT functions are distributed between a signal processor 210 and a linefeed driver 220. Signal processor 210 is responsible for at least the battery feed control, ringing control, supervision, codec, and hybrid functions. Signal processor 210 controls and interprets the large signal subscriber loop control signals as well as handling the small signal analog voiceband signals and the digital voiceband data. In one embodiment, the signal processor 210 is an integrated circuit.

In one embodiment, the signal processor includes a processor interface 214 to enable programmatic control of the signal processor 210. The processor interface effectively enables programmatic or dynamic control of battery control, battery feed state control, voiceband signal amplification and level shifting, longitudinal balance, ringing currents, and other subscriber loop control parameters as well as setting thresholds such as a ring trip detection thresholds and an off-hook detection threshold.

Signal processor 210 includes a codec for bi-directional transformation of the voiceband communications between the digital and analog domains as is well known in the art. The digital voiceband data is received from the digital switching network on interface 216. Within the signal processor, the digital voiceband data is coupled to a digital codec interface. An analog codec interface provides outgoing analog voiceband signals to the linefeed driver. The analog codec interface also receives incoming analog voiceband signals from the linefeed driver. The terms "incoming" and "outgoing" used in reference to the

voiceband (i.e., audio) signal refer to the intended data flow from the perspective of the digital switching network. Thus, incoming voiceband signals received from the subscriber line are transformed from analog to digital form and provided to the digital switching network. Outgoing voiceband signals from the digital switching network are transformed from digital to analog form and provided to the subscriber line for use by the subscriber equipment.

Signal processor 210 receives subscriber line state information from linefeed driver 220 as indicated by tip/ring sense 222. This information is used to generate control signals for linefeed driver 220 as indicated by linefeed driver control 212. In one embodiment, the linefeed driver control and outgoing analog voiceband signals are communicated on the same signal lines 212. Incoming analog voiceband signals are received by the signal processor on line 230.

Linefeed driver 220 maintains responsibility for battery feed to tip 280 and ring 290. Overvoltage protection is not explicitly illustrated, however, overvoltage protection can be provided by fuses and/or a network of clamping devices incorporated into linefeed driver 220, if desired. Linefeed driver 220 includes sense circuitry to provide signal processor 210 with pre-determined sensed subscriber loop operating parameters as indicated by tip/ring sense 222. Signal processor 210 performs any necessary processing on the sensed parameters in order to determine the operational state of the subscriber loop. For example, differences or sums of sensed voltages and currents are performed as necessary by signal processor 210 rather than linefeed driver 220. Thus common mode

and differential mode components (e.g., voltage and current) of the subscriber loop are calculated by the signal processor rather than the linefeed driver.

Linefeed driver 220 modifies the large signal tip and ring operating conditions in response to linefeed driver control 212 provided by signal processor 210. This arrangement enables the signal processor to perform processing as needed to handle the majority of the BORSCHT functions. For example, the supervisory functions of ring trip, ground key, and off-hook detection can be determined by signal processor 210 based on operating parameters provided by tip/ring sense 222.

Figure 3 illustrates one embodiment of the large signal linefeed driver circuitry for controlling tip and ring line voltages. Operational amplifier 320 controls the tip 380 portion of the subscriber line. Operational amplifier 330 controls the ring 390 portion of the subscriber line. Operational amplifiers 320 and 330 drive the tip 380 and ring 390 lines in accordance with linefeed control signals 310.

As illustrated in Figure 3, operational amplifiers typically use V_{DD} (approximately 5 VDC) or ground for the positive rail supply voltage and V_{BAT} (-24 to -75 VDC) for the negative rail supply voltage. Thus the amplifiers are relatively high voltage amplifiers. Moreover, due to the potential difference between V_{DD} and V_{BAT}, the operational amplifier bias currents result in non-negligible power consumption. Due to subscriber loop operational specifications, operational amplifiers 320 and 330 must be matched over a relatively large operating voltage range. The operational amplifiers are frequently constructed on a shared substrate within a high voltage integrated circuit in part to

facilitate matching. The dual high voltage precision operational amplifier approach tends to result in increased costs for the SLIC.

Figure 4 illustrates an alternative SLIC linefeed driver 410. In one embodiment, the linefeed driver 410 is implemented as a number of discrete components. Linefeed driver 410 includes voiceband sensing circuitry 420 and power circuitry 440.

Voiceband circuitry 420 enables retrieval of voiceband communications from the subscriber loop. Nodes 424 and 428 serve to communicate voiceband signals from the subscriber loop to signal processor 210 (i.e., "incoming audio"). Capacitors CR and CT effectively provide AC coupling for the incoming audio signal from the subscriber loop to the signal processor while decoupling signal processor 210 from the DC offsets of the tip 480 and ring 490 nodes. Thus capacitors CR and CT effectively provide DC isolation of the incoming analog audio interface formed by nodes 424 and 428 from the subscriber loop. In the embodiment illustrated, voiceband circuitry 420 provides AC coupling of the incoming analog audio signal between the subscriber loop and the signal processor using only passive components.

Power circuitry 440 provides the battery feed and other relatively high voltage functions to the subscriber loop in accordance with analog linefeed control signals provided by the signal processor 210 at nodes 442, 444, 446, and 448. These control signals act as pull-up/pull-down controls to manipulate the tip and ring currents. Processing of the sensed parameters of the tip and ring lines for generating the linefeed control signals is handled exclusively by signal processor 210.

The subscriber loop current and the tip and ring voltages are controlled by transistors Q1-Q6. Transistors Q1-Q4 are coupled in a common base configuration. Transistors Q5-Q6 are coupled in a common emitter configuration. The common base/common emitter combination isolates the low voltage circuitry of the signal processor from the high voltage of the subscriber loop while providing pull-down current capabilities into the battery feed.

Transistors Q5-Q6 function as pull-down circuitry to enable decreasing the tip and ring currents. Transistors Q1-Q4 serve as a control isolation stage to provide the control signals from the low voltage domain of the signal processor to the high voltage domain of the pull-down circuitry and the subscriber line. The voltage domain of the signal processor is approximately 0-5.0 volts. The voltage domain of the pull-down circuitry is approximately $-V_{BAT}$ to 0.0 volts. Due to the transistor junctions between the signal ground and the remainder of the pull-down circuitry, the voltage domains of the signal processor and the pull-down circuitry will not intersect during normal operation.

In one embodiment, Q1-Q4 are PNP bipolar junction transistors and Q5-Q6 are NPN bipolar junction transistors. Given that the base terminals of Q1-Q4 are coupled to ground, nodes 442-448 need only be approximately 0.7 volts to turn on transistors Q1-Q4. Due to the small voltage drop between the base and emitters of Q1-Q4, control of the linefeed circuitry requires relatively low power and thus linefeed driver control currents I1-I4 may be provided by a signal processor 210 implemented as a low voltage complementary metal oxide semiconductor (CMOS) integrated circuit.

Transistors Q1, Q4, and Q6 (and resistor R2) control the tip voltage 480. The tip voltage is increased by the application of control current I1 to Q1. The tip voltage (node 480) is decreased by the application of control current I4 to Q4. Control currents I1 and I4 provide pull-up and pull-down tip control signals for manipulating the tip voltage at node 480.

Similarly, transistors Q2, Q3, and Q5 (and resistor R1) control the ring voltage 490. The application of control current I3 to Q3 increases the ring voltage. Thus I3 represents the pull-up control signal for the ring voltage. The ring voltage is decreased by the application of control current I2 to Q2. Control current I2 is the ring voltage pull-down control signal. Control currents I2 and I3 provide pull-down and pull-up ring control signals for manipulating the ring voltage at node 490.

Control currents I1-I4 thus control the large signal subscriber loop current and tip and ring voltages. For example, the ringing signal can be generated by using the control signals at nodes 442-448 to periodically reverse the polarity of tip 480 with respect to ring 490 (i.e., battery polarity reversal) at the nominal ringing frequency.

Transistors Q1-Q6 are selected to have sufficiently high betas so that base currents are negligible. Thus the tip current (I_{TIP}) can be approximated as $I_{TIP} = I1 - I_{EQ6}$. The pull-up and pull-down controls are operated in a substantially mutually exclusive manner such that only one of I1 or I4 is nonzero at given point in time. The tip current is thus either I1 or $-I_{EQ6}$. As a result, the tip current can be determined indirectly by sensing the emitter current of transistor Q6. The ring current is either I3 or $-I_{EQ5}$ and can be

determined indirectly by sensing the emitter current of Q5. The tip and ring currents can thus be determined without direct sensing of the tip and ring lines.

Power circuitry 440 includes line sensing circuitry to enable determination of currents I_{EQ5} and I_{EQ6}. The line sensing circuitry includes sense resistor RR located in the emitter path of Q5 between the emitter of Q5 and V_{BAT} and sense resistor RT located in the emitter path of Q6 between the emitter of Q6 and V_{BAT}. Resistors RT and RR are used as sense impedances to generate a voltage drop (e.g.,V_{EQ6}-V_{BAT} and V_{EQ5}-V_{BAT}) for determining I_{EQ6} and I_{EQ5}. The voltage drop across RT is sensed using resistors RS1 and RS3. The voltage drop across RR is sensed using RS2 and RS3. Resistors RS1, RS2, and RS3 convert the voltages at nodes V_{EQ5}, V_{EQ6}, and V_{BAT} into sense currents IS1, IS2, and IS3, respectively, for processing by signal processor 210. In one embodiment, the line sensing circuitry consists only of passive discrete components.

Referring to Figures 2 and 4, tip/ring sense 222 includes the sensed currents IS1, IS2, and IS3 for determination of I_{EQ6}. Currents IS1, IS2, and IS3 are provided to nodes 432, 434, and 436 so that the signal processor can perform the appropriate calculations to control the tip and ring currents from the sensed currents. The sensed parameters (IS1, IS2, and IS3) enable the signal processor 210 to determine the subscriber loop common mode and differential mode currents. Generally, the tip and ring currents or the departure from the desired tip and ring currents is determined indirectly in the low voltage domain of the signal processor without directly sensing the high voltage, high current tip and ring lines. Thus resistors RS1, RS2, and RS3 form a sense or feedback isolation stage to

enable providing sensed parameters from the high voltage, high current domain of the power circuitry to the low voltage domain of the signal processor.

The voltage across the emitter resistor RT is proportional to the current flowing in the emitter of Q6. In particular,

$$V_{EQ6} - V_{BAT} = I_{EQ6} \bullet RT$$

Assuming RS1 and RS2 are significantly larger than emitter resistors RR and RT (and RS1≈RS3 and the nodal voltages V_{432}, V_{434}, and V_{436} are substantially the same), the difference in sense currents IS1 and IS3 represents a measure of I_{EQ6} in accordance with the equation:

$$I_{EQ6} = (IS3 - IS1) \bullet \frac{RS1}{RT}$$

Similarly,

$$I_{EQ5} = (IS3 - IS2) \bullet \frac{RS1}{RR}$$

Figure 5 illustrates low voltage tip/ring current differencing and mirroring circuitry 550 that may be incorporated into signal processor 210 for determining currents I_{EQ6} and I_{EQ5}. Operational amplifier 510 and transistors M1, M2, and M3 are used to invert and mirror IS3 to enable calculating the difference between currents IS1 and IS3 as well as the difference between IS2 and IS3. Operational amplifier 520 provides a tip sense signal 580 indicative of the current I_{EQ6} flowing through the emitter of Q6. Similarly operational amplifier 530 provides a ring sense signal 590 indicative of the current I_{EQ5} flowing through the emitter of Q5. Assuming a high beta (β) for Q5 and Q6, these emitter currents represent the subscriber line tip and ring pull-down currents. If the pull-up and

pull-down control signals are operated mutually exclusively in a push-pull fashion, the pull-down currents (when non-zero) represent the tip and ring currents (allowing for a change of sign).

Operational amplifier 510 provides a virtual short circuit terminating one end of resistor RS3 at a potential voltage equivalent to V_{REF} due to the presence of V_{REF} at the inverting input of operational amplifier 510. If V_{REF} is signal ground, then RS3 is effectively terminated at a virtual ground.

Transistors M1 and M2 are coupled in a current mirror configuration such that current IS3 is mirrored through the drain of transistor M2. Similarly transistor M3 is coupled in a current mirror configuration with transistor M1 to provide current IS3 through the drain of transistor M3.

Operational amplifier 520 is a transimpedance amplifier that forces the difference between IS3 and IS1 to flow across feedback resistor RFT. As long as V_{REF} at the inverting input of amplifier 510 is the same as V_{REF} at the noninverting input of operational amplifier 520, operational amplifier 520 effectively generates a signal corresponding to the difference between IS1 and IS3. The difference between these currents is proportional to the emitter current through transistor Q6 (i.e., $I_{EQ6} \propto IS3 - IS1$). Thus the voltage produced as the tip sense signal 580 is proportional to I_{EQ6} (i.e., $V_{580} \propto RFT \bullet I_{EQ6}$).

Transimpedance amplifier 530 similarly generates a ring sense voltage 590 proportional to the difference between IS2 and IS3. The difference between these currents is proportional to the emitter current through transistor Q5 (i.e.,

$I_{EQ5} \propto IS3 - IS2$). Thus the ring sense voltage V_{590} is proportional to I_{EQ5} (i.e., $V_{590} \propto RFR \bullet I_{EQ5}$).

Figure 6 illustrates the current differencing and mirroring circuitry 550 in block form as tip/ring sense circuitry 650 within signal processor 610. In one embodiment, amplifiers 624 and 634 are transconductance amplifiers for converting voltage levels corresponding to desired tip and ring currents into tip and ring pull-up currents I1 and I3. When non-zero, the tip and ring pull-up currents also correspond to the desired tip and ring currents.

The tip sense signal 680 is compared with a signal 622 corresponding to the desired tip current. Differential amplifier 620 generates a tip error signal ε_{TIP} as feedback for the tip pull-down control 660. Tip pull-down control 660 varies I4 in response to ε_{TIP}. Generally, when the actual tip current falls below the desired tip current, tip pull-up current I1 is applied. When the actual tip current exceeds the desired tip current, I4 is applied to increase the pull-down current I_{EQ5}. In one embodiment, tip and ring pull-down controls 660 and 670 are transconductance amplifiers.

The ring sense signal 690 is similarly compared with a signal 632 corresponding to the desired ring current. Differential amplifier 630 generates a ring error signal ε_{RING} as feedback for the ring pull-down control 670. Ring pull-down control 670 varies control currents I2 in response to ε_{RING}. When the actual ring current falls below the desired ring current, ring pull-up current I3 is applied. When the actual ring current exceeds the desired ring current, I2 is applied to increase the pull-down current I_{EQ6}.

Referring to Figure 4, the values of the impedances embodied by R1 and R2 may be selected to achieve the desired frequency response and current transfer characteristics between the control currents I1-I4 and the emitter currents I_{EQ5} and I_{EQ6}. In alternative embodiments the impedances may comprise, for example, passive networks of resistors and capacitors, or active components rather than single resistors R1 and R2 as illustrated.

The line sensing circuitry enables signal processor 210 to determine the large signal state of the subscriber loop without the need for intervening active circuitry or level shifters. The line sensing circuitry allows sensing of the high voltage circuitry by the low voltage signal processor. The tip and ring error signals are generated in the low voltage domain of the signal processor. The common base/common emitter configuration isolates the low voltage signal processor from the high voltages of the subscriber line while providing pull-down current capabilities into the battery feed. In one embodiment, the signal processor resides in a low voltage integrated circuit package and the linefeed control circuitry is external to that package such that the signal processor and linefeed control circuitry do not reside on a same semiconductor substrate.

In one embodiment, the line sensing circuitry comprises only passive discrete components. The linefeed control inputs 442-448 enable signal processor 210 to actively manage the large signal state of the subscriber loop. The large signal AC and DC control loops are effectively terminated at the signal processor 210. In particular, the large signal AC and DC components of the subscriber loop control protocol can now be controlled directly by a low voltage integrated circuit. Signal processing and state determination such as off-hook, ring trip, and ring control formerly associated with high power analog

circuitry can be handled predominately by the low voltage integrated circuit. In addition, the integrated circuit signal processor can handle processing of the small signal analog voiceband signals from the subscriber loop without the need for intervening active elements or level shifting circuitry.

In one embodiment, the outgoing analog audio signal is superimposed on the control currents I1 and I3 for power circuitry 440. Thus the outgoing audio signal and the linefeed control signals are provided on the same signal lines to the linefeed driver circuitry. The outgoing audio signal is communicated using nodes 442 and 446. One advantage of this configuration is that the termination impedance can be set by controlling currents I1 and I3. The use of a programmable signal processor effectively places the value of the termination impedance under programmatic control.

Transistors Q1 and Q3 are coupled in a common base configuration. Transistors Q1 and Q3 couple the outgoing audio signal received from the signal processor. In one embodiment, an audio current source manipulates I1 and I3 to put the outgoing audio signal onto the tip 480 and ring 490 nodes. This can be accomplished, for example, by superimposing the audio signal current source on the large signal control currents provided by tip control 660 and ring control 670. The common base isolation stage effectively isolates the signal processor from the DC offset of the tip 480 and ring 490 nodes.

A DC bias current is established in Q1 and Q3 with non-precision low voltage and high voltage circuitry. The DC bias does not directly affect the audio gain or balance and thus high precision is not required. Subscriber line impedance synthesis can be accomplished by providing sensed tip and ring voltages as feedback for the audio current

source. Greater gain and balance control can be achieved through the use of transistors with higher or better matched betas. Alternatively, other configurations such as Darlington pairs can be used to achieve a greater beta. Different types of transistors such as metal oxide semiconductor or junction field effect transistors (i.e., MOSFET or JFET) can be used for either the common base isolation stage (Q1-Q4) or the drive transistors (Q5-Q6) in alternative embodiments. The term "common base" includes "common gate" equivalents for MOSFET and JFET transistors. Thus a "common base isolation stage" is intended to include field effect transistors coupled in a common gate configuration.

In the preceding detailed description, the invention is described with reference to specific exemplary embodiments thereof. Various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method comprising the steps of:

a) providing subscriber loop pull-down circuitry operating in a first voltage domain, wherein the subscriber loop pull-down circuitry decreases at least one of a tip and a ring line current in response to a corresponding pull-down control signal; and

b) providing control circuitry operating in a second voltage domain wherein the first and second voltage domains are substantially distinct, wherein the control circuitry varies the pull-down control signal in response to a sensed current corresponding to an associated one of a tip pull-down current and a ring pull-down current.

2. The method of claim 1 further comprising the steps of:

c) providing pull-up circuitry, wherein the pull-up circuitry increases the at least one of the tip and ring currents in response to a corresponding pull-up control signal provided by the control circuitry.

3. The method of claim 2 wherein for each of the tip and ring lines, the pull-up and pull-down control signals are mutually exclusive such that the control circuitry does not provide a pull-up and a pull-down control signal for a selected line substantially simultaneously.

4. The method of claim 1 further comprising the step of

c) providing a feedback isolation stage, wherein the feedback isolation stage converts voltages sensed at each end of a tip sense impedance and a ring sense impedance into first and second currents, wherein the sensed current for a selected one of the tip and ring lines represents a difference between the first and second currents for the corresponding selected one of the tip and ring sense impedances, wherein a difference between the first and second currents for each of the tip and ring lines is calculated in the second voltage domain.

5. The method of claim 1 further comprising the step of:

c) providing a control isolation stage, wherein the control isolation stage provides the pull-down control signals from the control circuitry operating in the second voltage domain to the pull-down circuitry operating in the first voltage domain.

6. A subscriber line interface circuit apparatus, comprising:

pull-down circuitry operating in a first voltage domain, wherein the pull-down circuitry varies a current of a selected one of a tip and a ring line in response to a pull-down control signal;

control circuitry providing the pull-down control signal, the control circuitry operating in a second voltage domain substantially distinct from the first voltage domain;

a control isolation stage coupled to provide the pull-down control signal from the control circuitry to the pull-down circuitry; and

a feedback isolation stage providing feedback signals from the pull-down circuitry to the control circuitry, wherein the feedback signals represent a sensed pull-down current associated with the selected line , wherein the control circuitry provides the pull-down control signal for the selected line in response to the sensed pull-down current.

7. The apparatus of claim 6 wherein the pull-down circuitry further comprises:

a first pull-down transistor having a first terminal coupled to the selected line of the subscriber line and a second terminal coupled to a battery feed node through a first sense impedance, wherein a first sense impedance current is the sensed pull-down current.

8. The apparatus of claim 7 wherein the sense impedance comprises a resistor.

9. The apparatus of claim 8 wherein the sense impedance further comprises a capacitor.

10. The apparatus of claim 7 wherein the sense impedance consists of passive components.

11. The apparatus of claim 6 wherein the feedback isolation stage consists of passive components.

12. The apparatus of claim 11 wherein the feedback isolation stage comprises resistors.

13. The apparatus of claim 6 wherein the control isolation stage comprises active components.

14. The apparatus of claim 13 wherein the active components are coupled in a common base configuration.

15. The apparatus of claim 13 wherein the active components comprise bipolar junction transistors coupled in common base configuration.

16. The apparatus of claim 13 wherein the active components comprise field effect transistors coupled in common gate configuration.

17. An apparatus, comprising:

a current mirror providing an inverted first sense current from a received first sense current; and

a transimpedance amplifier coupled to receive the inverted first current and a second current, the transimpedance amplifier providing a sense signal proportional to a difference between the first and second sense currents, wherein the sense signal is proportional to a pull-down current flowing into a battery feed node of a subscriber loop,

wherein the pull-down current is approximately the same as one of the subscriber loop tip and ring currents associated with the first and second currents.

18. The apparatus of claim 17 further comprising:

a differential amplifier providing an error signal indicative of a difference between the sense signal and a desired signal; and

a linefeed driver control circuit providing a pull-down control signal to vary the associated one of the tip and ring currents of the subscriber loop in response to the error signal.

19. A subscriber line interface circuit apparatus comprising:

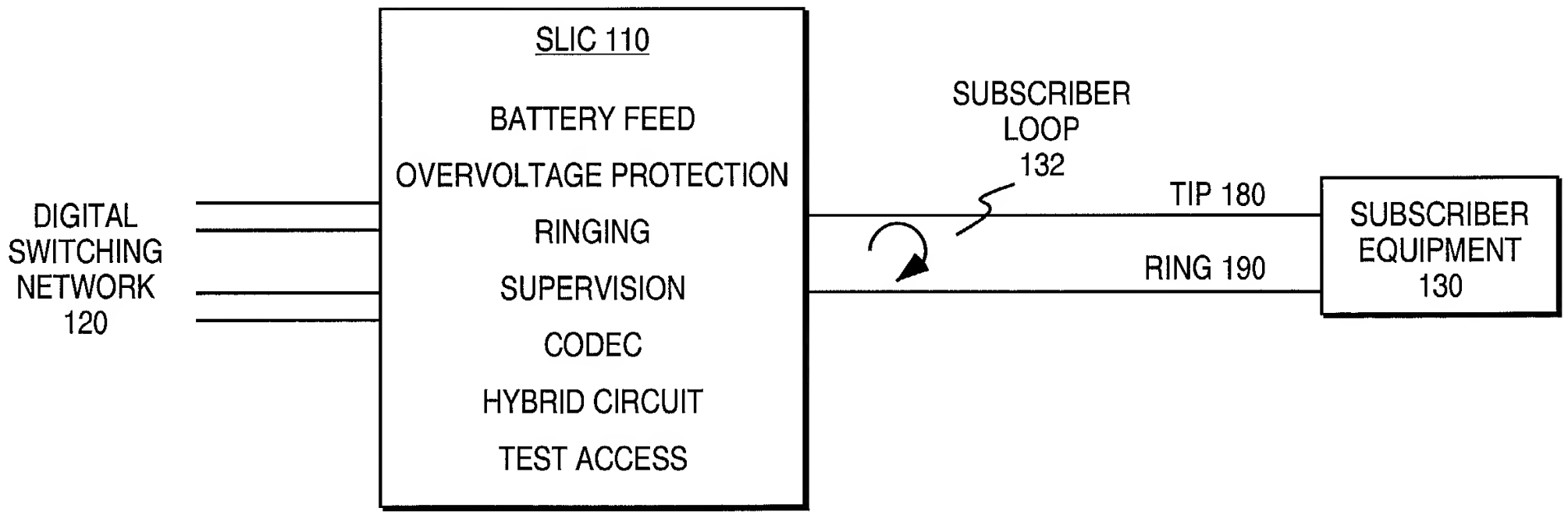
a linefeed driver responsive to pull-up and pull-down control signals to vary at least a selected one of a tip and a ring current of a subscriber loop; and

a signal processor sensing a pull-down current of the selected one of the tip and ring lines into a battery feed node, the signal processor generating pull-down control signals for the selected current in response to the sensed pull-down current, wherein the linefeed driver does not reside within a same integrated circuit package as the signal processor.

20. The apparatus of claim 19 wherein the signal processor calculates the selected current without directly sensing either the tip or ring lines of the subscriber loop.

ABSTRACT OF THE DISCLOSURE

A method includes the step of providing subscriber loop pull-down circuitry operating in a first voltage domain. The subscriber loop pull-down circuitry decreases at least one of a tip and a ring line current in response to a corresponding pull-down control signal. The method further includes the step of providing control circuitry operating in a second voltage domain, wherein the first and second voltage domains are substantially distinct. The control circuitry varies the pull-down control signal to decrease a selected one of the tip and ring line currents in response to a sensed current corresponding to an associated one of a tip pull-down current and a ring pull-down current. A subscriber line interface circuit apparatus includes pull-down circuitry operating in a first voltage domain. The pull-down circuitry varies line currents of the tip and ring lines in response to a pull-down control signal provided by control circuitry operating in a second voltage domain. The first and second voltage domains are substantially distinct. A control isolation stage is coupled to provide the pull-down control signals from the control circuitry to the pull-down circuitry. A feedback isolation stage provides feedback signals from the pull-down circuitry to the control circuitry. The feedback signals represent sensed pull-down currents associated with the tip and ring lines. The control circuitry provides the pull-down control signals for the tip and ring lines in response to the sensed pull-down currents.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SUPERVISION
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TEST ACCESS
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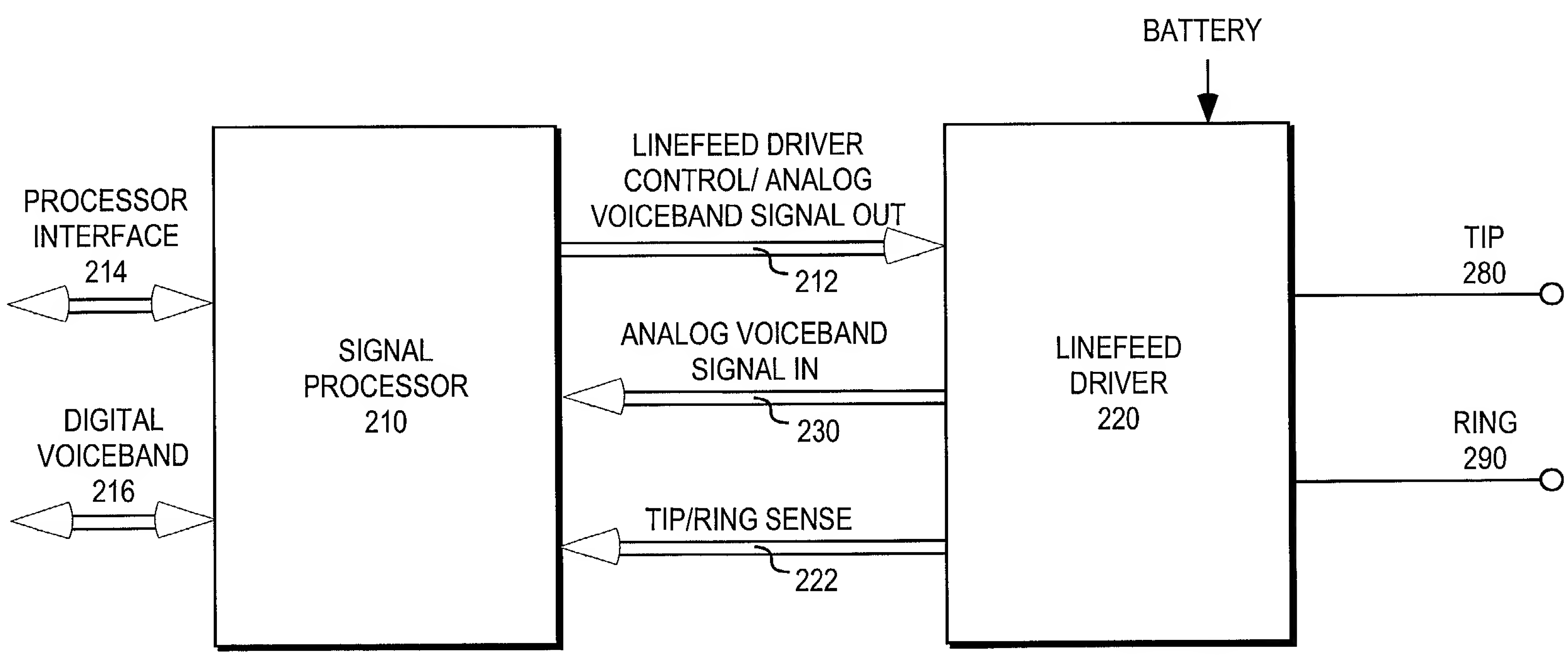
TIP 180
RING 190
SUBSCRIBER EQUIPMENT 130

FIG. 1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DIGITAL
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SIGNAL
PROCESSOR
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VOICEBAND SIGNAL OUT
212
ANALOG VOICEBAND
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222
BATTERY
LINEFEED
DRIVER
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TIP
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RING
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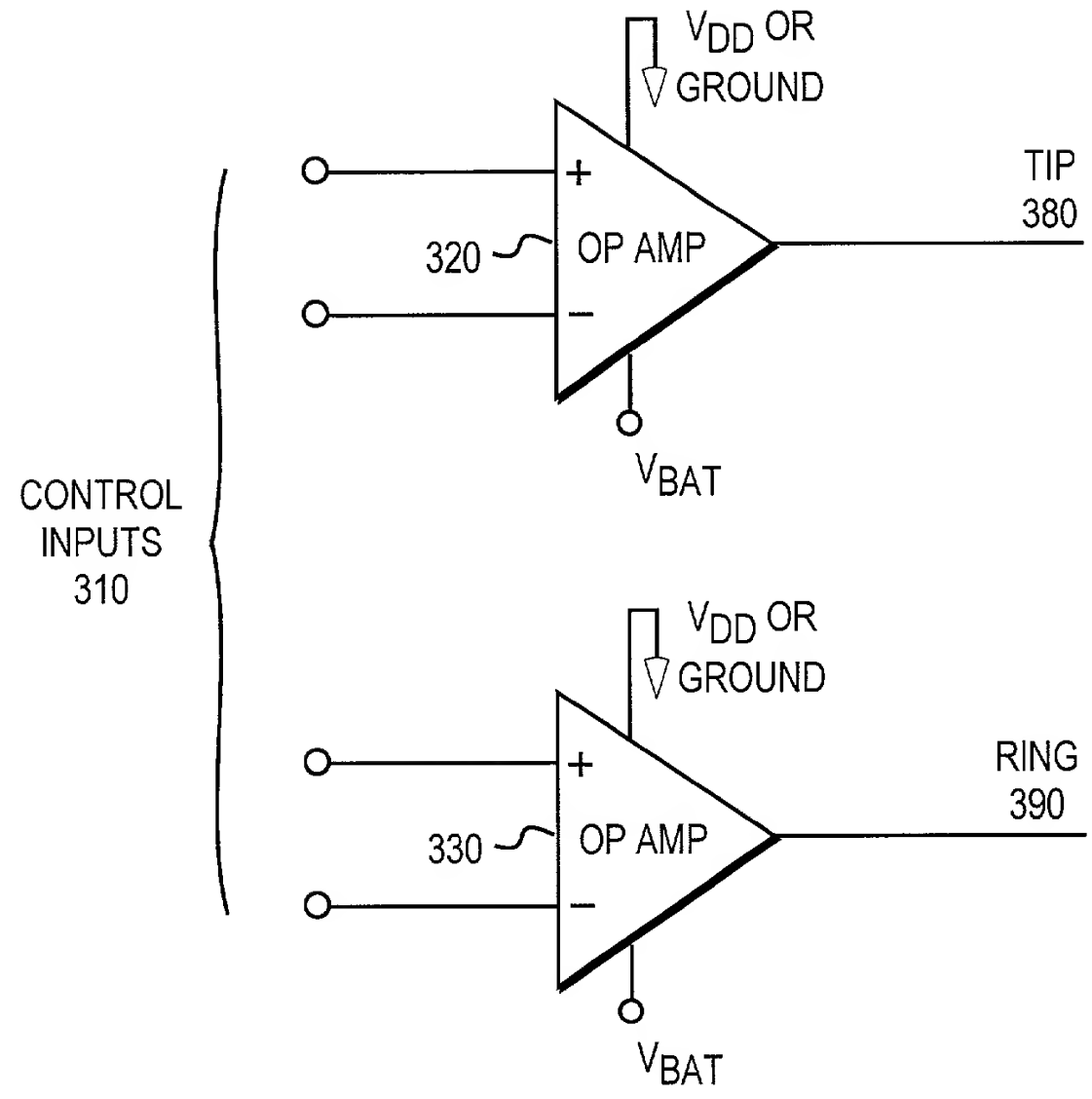
FIG. 2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GROUND
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TIP
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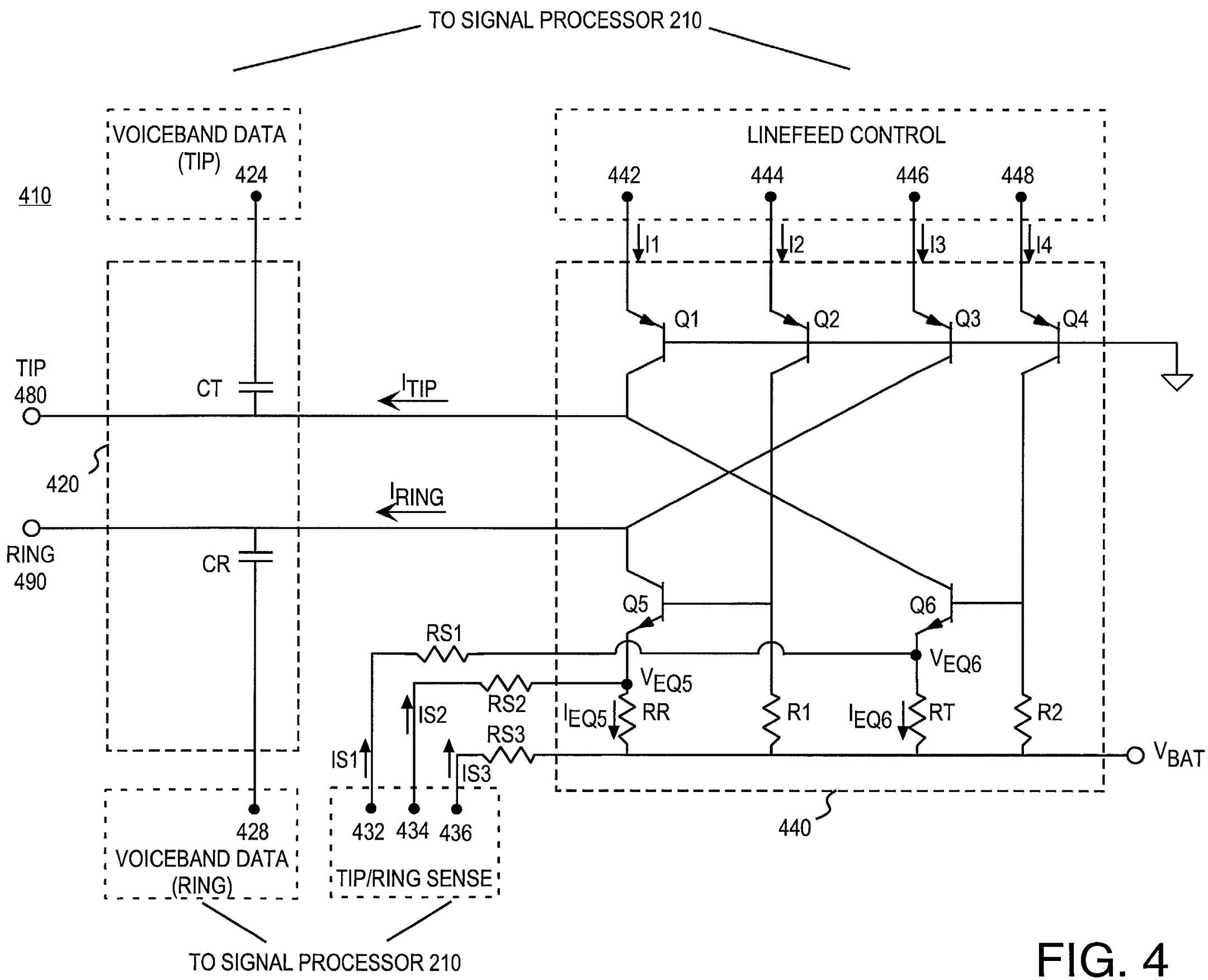
+
−
RING
390
V_{BAT}

FIG. 3


TO SIGNAL PROCESSOR 210
VOICEBAND DATA
(TIP)
424
410
LINEFEED CONTROL
442
444
446
448
I1
I2
I3
I4
Q1
Q2
Q3
Q4
TIP
480
CT
ITIP
420
IRING
RING
490
CR
Q5
Q6
RS1
VEQ6
VEQ5
RS2
IS2
IEQ5
RR
R1
IEQ6
RT
R2
RS3
IS1
IS3
VBAT
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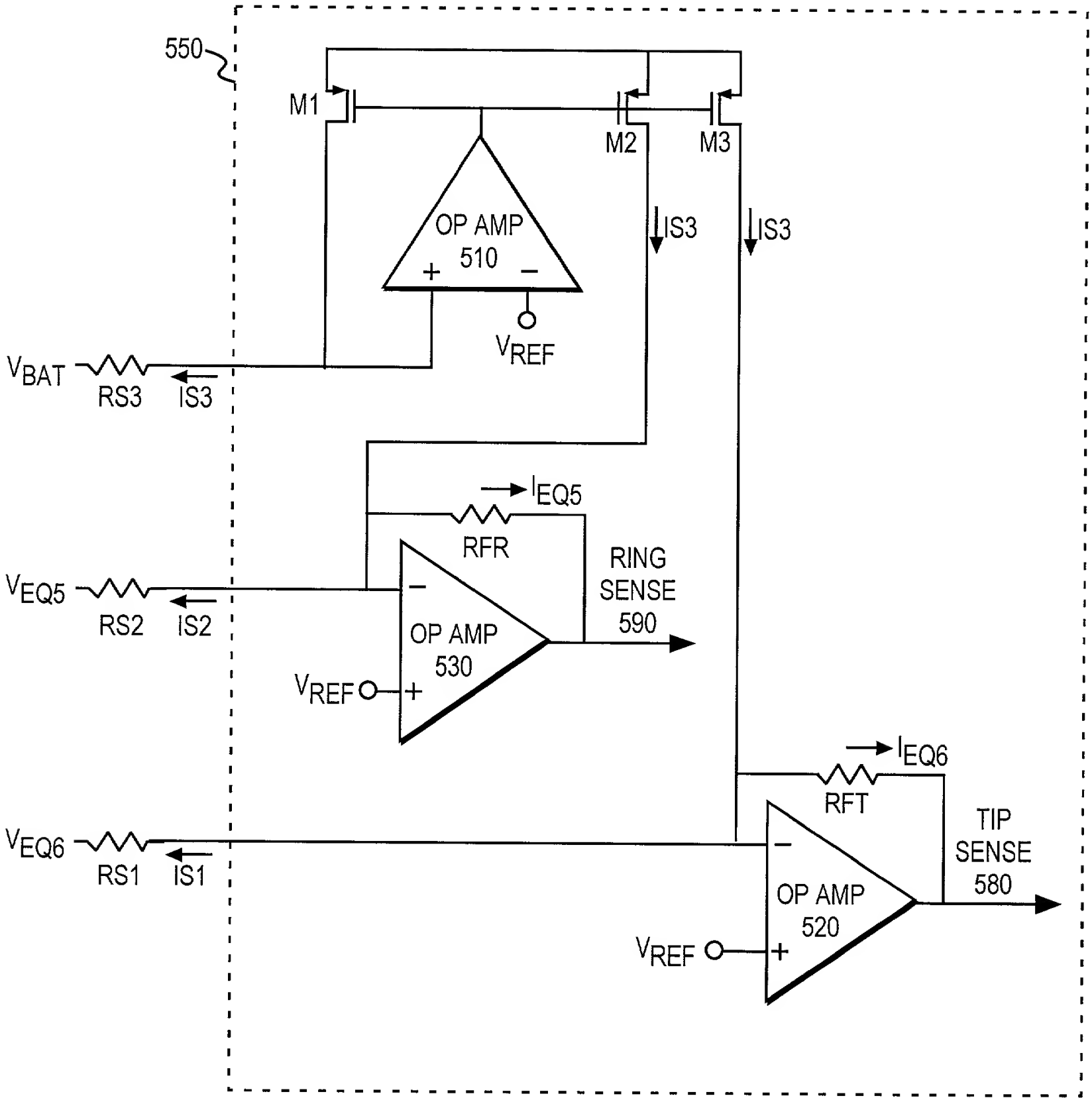
428
432
434
436
VOICEBAND DATA
(RING)
TIP/RING SENSE
TO SIGNAL PROCESSOR 210

FIG. 4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M2
M3
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RS2
IS2
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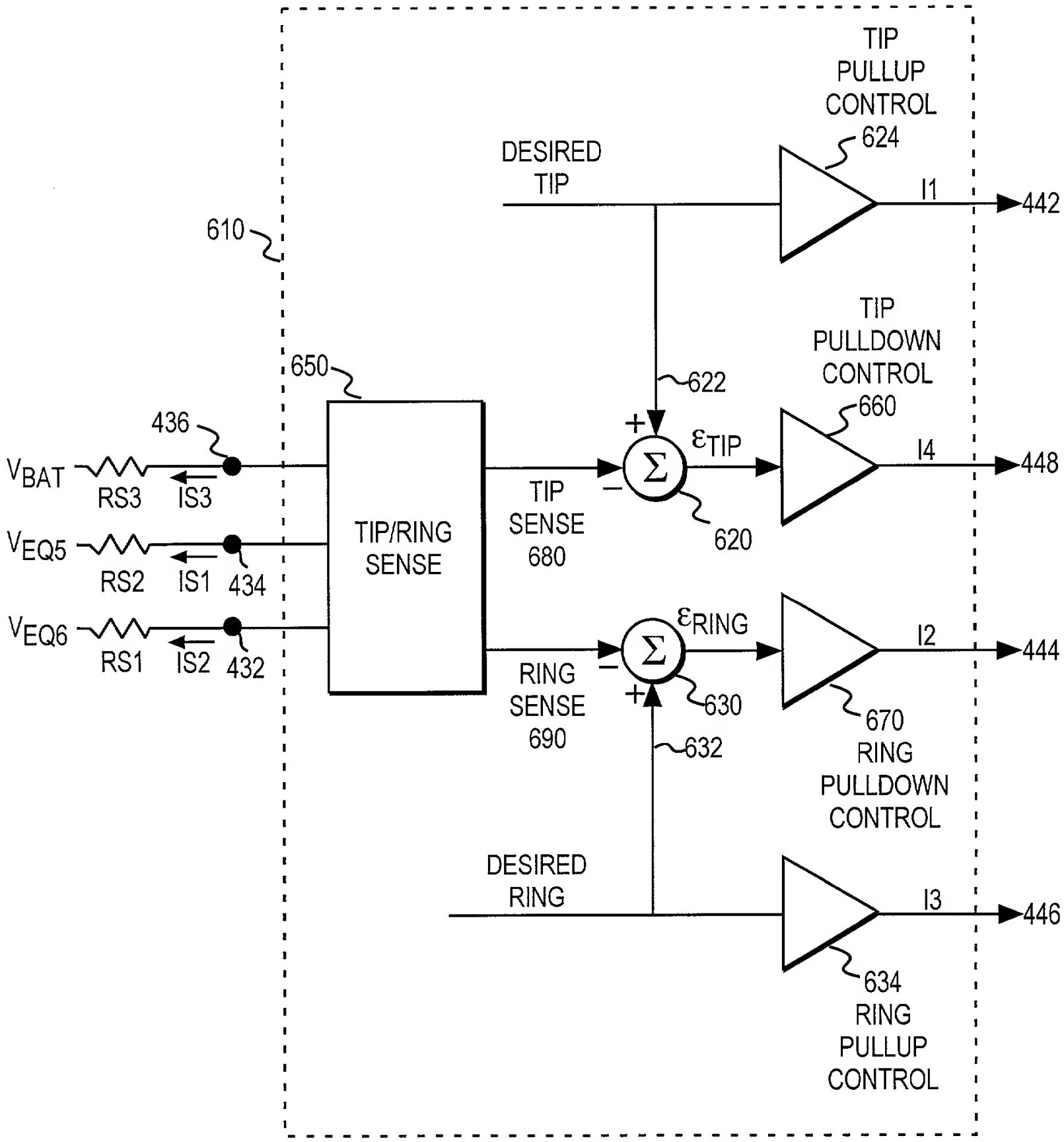
FIG. 5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TIP/RING SENSE
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RS3
IS3
V_{EQ5}
RS2
IS1
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432
DESIRED TIP
TIP PULLUP CONTROL
624
I1
442
622
TIP PULLDOWN CONTROL
660
I4
448
ε_{TIP}
TIP SENSE 680
620
ε_{RING}
RING SENSE 690
630
632
I2
444
670
RING PULLDOWN CONTROL
DESIRED RING
I3
446
634
RING PULLUP CONTROL

FIG. 6

DECLARATION/POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

LOW VOLTAGE SENSING AND CONTROL OF BATTERY REFERENCED TRANSISTORS IN SUBSCRIBER LOOP APPLICATIONS

the specification of which

__X__ is attached hereto.
_____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Foreign Application(s) and/or Claim of Foreign Priority
I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Country	Application No.	Date Filed	35 U.S.C. §119 Priority Claimed

Provisional Application Claim of Priority
I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Filing Date	Status

Power of Attorney

I hereby appoint the following attorney(s) and/or agent(s) with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

William D. Davis, Reg. No. 38,428; and Bruce A. Johnson, Reg. No. 37,361 of Davis & Johnson, L.L.P., P.O. Box 90698, Austin, Texas 78709 Telephone: (512) 858-1218

Correspondence Address

Send Correspondence To:	Direct Telephone Calls to:
William D. Davis Davis & Johnson, L.L.P. P.O. Box 90698 Austin, TX 78709	William D. Davis (916) 364-1270

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First Inventor: Jerrell P. Hein **Citizenship: USA**
Residence Address: 19507 FM 150 West, Driftwood, Texas 78619
Post Office Address: same

Inventor's Signature _____ **Date** 10/20/00

Full Name of Second Inventor: Marius Goldenberg **Citizenship: USA**
Residence Address: 9300 Edwardson Lane, Austin, Texas 78749
Post Office Address: same

Inventor's Signature _____ **Date** 10/20/00